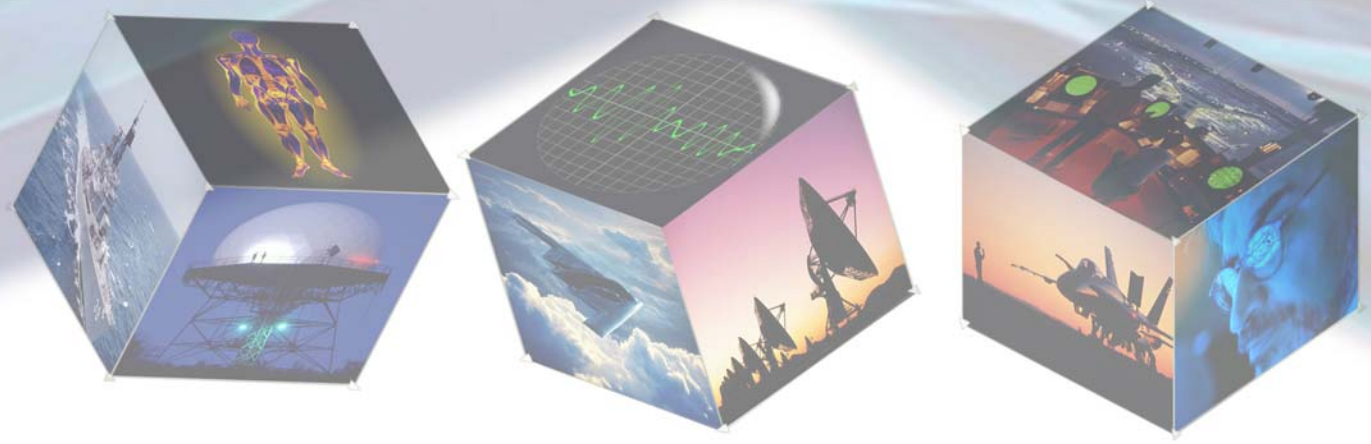
GETTING STARTED GUIDE

MODEL 71760

4–Channel 200 MHz A/D
Onyx® Family XMC Module



PENTEK

Setting the Standard for
Digital Signal Processing

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Manual Revision History

Date	Revision	Comments
7/25/13	1.0	Initial Release
12/18/13	1.1	Revised What's in the Box?

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What's in the Box?

Your shipment of the Pentek Model 71760 should include the items on the following list. If anything is missing or damaged, contact Pentek immediately at (201) 818−5900. Please save the shipping container and packing material in case reshipment is required.

Quantity	Part Number	Description
1	002.71760	Model 71760 Board
1	002.71504	Terminator Board
1	174.50010	Battery (see Note below)
1	300.70001	Front Panel Gasket
3	353.02607	26−Pin Socket for Ribbon Cable (Sync)
2 feet	378.62602	26−Conductor Ribbon Cable, 30GA 025 (Sync)
2	356.00015	Shorting Plugs
4	385.30200	Mounting Screws (2.5x6mm Phillips).
1	808.71760	Instruction Manual Kit (all included manuals)

The list above includes all the standard parts that are shipped with the Pentek Model 71760. The options for this product are described in this *Getting Started Guide* and in the *Pentek Model 71760 Operating Manual* (included in the box).

NOTE: If you plan to use the FPGA bitstream encryption capability, such as with Pentek's Gateflow software, you must install the battery in the Model 71760's main PCB as shown in Section 2.5 of the *Pentek Model 71760 Operating Manual*.

Introduction

This document describes the Pentek Model 71760 Onyx® Family XMC module, its associated software, what to consider before installation, and installation steps.

Before You Begin: Description of Hardware

Pentek's Onyx Family Model 71760 is a multichannel, high−speed data converter. It includes four 200−MHz, 16−bit A/D converters. Model 71760 is compatible with the VITA 42.0 XMC format and supports PCIe Gen 1, 2, or 3 as a native interface.

The Model 71760 XMC module can be attached directly to any digital signal processing (DSP) baseboard equipped with an XMC expansion site, or to an XMC carrier/adaptor, such as the Pentek Model 7806 XMC PCI Express carrier.

Refer to the *Model 71760 Operating Manual* (800.71760) for a complete description of hardware operation and programming.

Before You Begin: Consider the Host Bus Characteristics

When you install Model 71760, you may need to set DIP switch **SW1**, which controls FPGA Configuration, based on the characteristics of your host bus. Therefore, you will need to consider the following before you begin installation:

- FLASH memory write protect/write enable
- PLX PCIe switch maximum speed select
- Select boot configuration at power on
- PCIe clock select
- P16 Clock select
- GateXpress disable

For example, Switch **SW1−2** allows you to change the maximum speed of the PLX PCIe switch from Gen 2 (the factory default) to Gen 3. To preview the DIP switch settings you'll need to make, refer to Section 2.2 of the *Model 71760 Operating Manual* (800.71760).

NOTE: Model 71760 is shipped to boot with the Gen 2 x8 PCIe default FPGA code. If you want a different default, see Section 2.2 of the *Model 71760 Operating Manua*l.

Before You Begin: Description of Software

Board Support Software for the Pentek Model 71760 XMC

Pentek's ReadyFlow® Board Support Packages (BSP) contain software support for the Model 71760 XMC. This includes a device driver for the 71760, plus the ReadyFlow Board Support Library data structures and routines. The following available BSPs allow high−level programming for various workstation platforms. Refer to the *User's Guide* indicated for each platform:

- Model 4994A Option 166 ReadyFlow BSP for Linux® (816.71660)
- Model 4995A Option 166 ReadyFlow BSP for Windows® (815.71660)

Pentek's ReadyFlow® Board Support Libraries contain a set of C−language routines for the Model 71760. Refer to the *Programmer's Reference* for the 71760 (801.71760).

Software for the FPGAs

The FPGA is supported with a Pentek GateFlow® FPGA Design Kit. The GateFlow Design Kit (Model 4953 Option 166) facilitates user−installed FPGA functions using the Xilinx ISE Design Suite. The FPGA Design Kit allows the user to modify, add to, or replace the default logic functions within the FPGA with functions of his or her own definition.

Note that GateFlow is a very specialized software package intended for users with experience in FPGA logic programming. This package may not be required if the default functions included in the FPGA code, as written by Pentek, satisfy the require−ments of your application.

Refer to the following GateFlow software documentation: *Pentek Model 4953−176 User Manual: Pentek Onyx Model 71760 GateFlow User Manual* (807.71760).

Before You Begin: Consider the Product's Options

Timing and Synchronization

The following timing and synchronization options are available for the Model 71760's A/D converters:

- **External sample clock:** Received from the front panel SSMC connector labeled **CLK**. The external clock signal must be a sine wave or square wave of +0 dBm to +10 dBm, with a frequency range from 10 to 800 MHz (must be divided down by CDCM7005 for ADC when greater than 200MHz). This input is enabled using the Sync Bus Control Register 1 CLK SEL bits (see the *Model 71760 Operating Manual*).

  NOTE: Ensure that the ADC clock never exceeds the ADS5485 rated clock speed during any change of frequency with the input clock signal. Refer to Section 2.7.1 of the *Model 71760 Operating Manual* for details.

- **Onboard crystal oscillator**: Alternately, the sample clock can be sourced from an onboard programmable voltage−controlled crystal oscillator (VCXO). In this mode, the front panel SSMC connector (labeled **CLK**) can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

- **26−pin sync bus front panel connector**: This connector (labeled **SYNC/GATE**) allows multiple modules to be synchronized. It provides clock, sync, and gate input/output pins for the Low−Voltage Positive Emitter−Coupled Logic (LVPECL) Sync Bus. When the Model 71760 is a bus Master, these pins output LVPECL Sync Bus signals to other slave units. When the Model 71760 is a bus Slave, these pins input LVPECL signals from a bus Master. This connector also accepts two Low−Voltage TTL (LVTTL) Gate/Sync inputs. The mating 26−pin connector is Pentek part # 353.02607 (ERNI # 214346). For a description of the **SYNC/GATE** connector pin configuration, refer to the *Model 71760 Operating Manual*.

- **External trigger input:** Received from the front panel SSMC coaxial connector, labeled **TRIG**. The external trigger signal must be an LVTTL signal. The trigger input can be used as a gate or trigger for A/D signal processing. This input is enabled using Sync Bus Control Register 2 TTL SRC bits (see the *Model 71760 Operating Manual*).

  NOTE: The front panel TTL Gate and Sync signals are 5V tolerant but they must **not** have any negative voltage applied. They are terminated with a 392−ohm resistor to 3.3V and a 392−ohm resistor to ground.

FPGA Digital Interfaces

Model 71760 includes a Xilinx Virtex–7 FPGA. The FPGA serves as a control and status engine with data and programming interfaces to each of the onboard resources including the A/D converters and RAM memory. The FPGA is factory programmed by Pentek to implement the standard signal processing and control functions specified in the *Model 71760 Operating Manual*. The Pentek GateFlow® FPGA Design Kit facilitates integration of user–created IP with the factory shipped functions.

Following are the options for custom I/O:

- **Option 104 adds PMC P14 LVDS connections to the FPGA** for custom I/O. This interface is configured by default as 8 LVDS input pairs, 8 LVDS output pairs, and 2 LVDS clock pairs. Note that while the Pentek–supplied FPGA code reserves pins and assigns signals to this interface, there is nothing in the code that drives or receives these signals. The GateFlow kit can be used to reconfigure the direction and/or logic levels of any or all of these signals, and to create functions to drive and/or receive them.

  NOTE: The **P14** signals can be configured in the FPGA as either LVDS or LVTTL but in either case are limited to 2.5V for the VX330T, or 1.8V for the VX690T, and also cannot be driven with a negative voltage.

- **Option 105 adds XMC P16 gigabit serial connections to the FPGA** for custom high–speed I/O.

FPGA Configurations

The Model 71760 includes a Xilinx Virtex–7 FPGA:

- Option 073 is a Xilinx XC7VX330T–2 FPGA
- Option 076 is a Xilinx XC7VX690T–2 FPGA

Model 71760 is shipped with a default FPGA configuration on FLASH memory. Model 71760 loads the FPGA configuration from FLASH memory at power–up. Up to four FPGA configurations can be stored in FLASH, identified as Version 0, Version 1, Version 2, and Version 3. The default FPGA configuration is located in the Version 0 space. The other three positions are empty.

The PCIe core is Gen 3 x8, and can negotiate down to Gen 2 or Gen 1 x4, as needed. While the board can support Gen 3, the board is shipped with the FPGA configuration SW (SW1–2) set to off, which limits the board to Gen 2. For more information, refer to Section 2.2 in the *Model 71760 Operating Manual*.

Documentation Required for Installation

NOTE: Some manuals are used for more than one Pentek product. The manuals listed below are all used for Model 71760.

- **Pentek Model 71760 Operating Manual** (800.71760): Describes the installation, operation, and programming of Model 71760.
- **Installation and Getting Started Guide for the Pentek ReadyFlow software** version for the workstation platform you're using (815.71660 for Windows, 816.71660 for Linux).
- **Pentek Model 4953–176 User Manual: Pentek Onyx Model 71760 GateFlow User Manual** (807.71760).

Step 1: Unpacking and Inspecting the Unit

After unpacking, inspect the unit carefully for possible damage to connectors or components. If anything is missing or damaged, contact Pentek immediately at (201) 818−5900. Please save the shipping container and packing material in case reshipment is required.

Step 2: Checking the Jumper and Switch Settings

At the factory, all DIP switches on the Model 71760 are installed in default positions. **The default parameters selected may or may not meet your requirements.**

As described above in Before You Begin: Consider the Host Bus Characteristics, the DIP switches set FPGA configuration. Before installing your Model 71760, **review Section 2.2 in the Model 71760 Operating Manual** to determine whether you need to change any settings.

NOTE: You should only change the DIP switches that are described in the *Model 71760 Operating Manual* − all others are reserved for factory use only.

Step 3: Installing the Hardware

Model 71760 mounts on the connector side of an XMC baseboard or carrier. To install the Model 71760, follow the procedure in Section 2.6 (Installing the Model 71760 on a XMC Baseboard) in the *Model 71760 Operating Manual*. Refer to the operating manual supplied with your baseboard for any specific mounting instructions.

NOTE: The JTAG PCB on the Model 71760 board is used for downloading new FPGA configuration code. If you do not plan to use the JTAG PCB, you can remove it before installing Model 71760. If you do plan to use the JTAG PCB, you should remove it before you deploy the Model 71760 board.

Step 4: Installing the Cabling

Connect a cable for each analog signal your application requires to the Model 71760's front panel SSMC socket receptacles. These are labeled **IN 1**, **2**, **3**, & **4**: one for each ADC input channel. The other cabling you install on the Model 71760's front panel depends on how you want to handle timing and synchronization (see Timing and Synchroniza−tion). Multiple boards can be synchronized via the 26−pin sync bus connectors (**SYNC**) using a ribbon cable. Systems requiring more synchronized channels can be supported with the Model 7190 Clock Synthesizer.

Step 5: Installing the Software

ReadyFlow Software

Pentek's ReadyFlow Libraries are software packages designed to provide software development tools for specific Pentek products on specific operating systems or plat–forms. The installation procedure is different for each platform:

Linux – The installation steps can be summarized as follows:

- Installing ReadyFlow in a Linux system
- Installing WinDriver (required to run example programs)
- Building the ReadyFlow example programs
- Building the ReadyFlow board support libraries

For complete details, refer to Chapter 2 of the *Model 4994A Option 166 User's Guide* (816.71660). Note that this document also supports Cobalt® (716xx) products.

Windows – You must install the Pentek ReadyFlow package BEFORE you attempt to boot the Model 71760 under Windows. The installation steps can be summarized as follows:

- Installing ReadyFlow in a Windows system
- Initializing the hardware (Model 71760) in Windows (responding to the New Hardware Wizard)
- Building the ReadyFlow example programs
- Building the ReadyFlow board support libraries

For complete details, refer to Chapter 2 of the *Model 4995A Option 166 User's Guide* (815.71660). Note that this document also supports Cobalt® (716xx) products.

GateFlow FPGA Design Kit

The following software and hardware is required to use the GateFlow FPGA Design Kit:

- **Xilinx's ISE Design Suite** (Version 14 or later): The GateFlow FPGA Design Kit was produced using the Xilinx ISE Design Suite Version 14.5, Application Version P.58f).

- **Flashload Utility:** This utility is supplied with the ReadyFlow software, but used with the GateFlow FPGA Design Kit as part of the process for implementing a project. The flashload utility reads a **`.mcs`** file, creating a binary image that is loaded into FLASH memory on the Model 71760 XMC module.

- **Pentek Model 71705 JTAG PCB:** This JTAG adaptor, which comes already installed on Model 71760 is used for downloading new configuration code. After completing the development of your changes to the standard Pentek factory−supplied configu−ration, you should remove the JTAG PCB from your Model 71760.

- **Xilinx's Platform Cable:** To connect to your development computer system you will need one of the following two cables, purchased from Xilinx:
    - Platform Cable USB (DLC−9, Xilinx part # HWUSB−G)
    - Platform Cable USB II (DLC10, Xilinx part # HWUSB−II−G)

  The Platform USB cable connects to a USB port on your development computer system, and thus carries its own 5V supply connection. The other end of both cables terminates in a pod, which contains a shrouded connector for a 14−pin, 2 mm pitch ribbon cable. The ribbon cable is included with the shipment of both Xilinx pro−gramming cables.

To install the FPGA Design Kit for the Model 71760's Processing FPGA, copy the **`\GateFlow`** folder on the DVD−ROM to the root directory of the C: drive of the system you'll be working on. Unzip the archived project files.

The directory structure of the GateFlow DVD−ROMs mimics that of the development system upon which the original projects were created. We recommend that you copy the **`\GateFlow`** folder on each DVD−ROM to the root directory of the C: drive of the sys−tem you'll be working on, such that the original, absolute pathnames of all files in the included project are maintained.

Full details for installing the FPGA Design Kit are provided in Chapter 1 of the Gate−Flow user manuals listed in Documentation Required for Installation.

Details about using flashload to download the **`.mcs`** file into the FLASH memory are provided in Chapter 2, Section 2.4.2 of the GateFlow user manual.

Step 6: Using the Software

ReadyFlow Software

The *User's Guide* for each ReadyFlow BSP provides instructions for using the Ready–Flow software. Chapter 3 provides the following:

- Introduction to ReadyFlow – Provides an overview of how the software is used.
- Using ReadyFlow – Provides details about using ReadyFlow, along with a modified code snippet from an example program.
- Using Linked Lists – Describes how to set up ADC Trigger Controller Linked Lists along with a code snippet from an example program.

Chapter 4 describes the ReadyFlow data structures and routines that access the Linux or Windows device driver functions.

Chapter 5 describes Command Line use and operation.

Chapter 6 describes Signal Analyzer use and operation.

GateFlow FPGA Design Kit

Chapter 2 of the *GateFlow User Manual* covers procedures for implementing a project:

- Using Your GateFlow FPGA Design Kit with Xilinx's ISE Design Suite Software
- Preparing for a New FPGA Configuration
- Transferring Configuration Data to the Model 71760

The GateFlow FPGA Design Kit includes test bench files and simulation projects that functionally simulate many operations of the Model 71760, when the FPGAs are con–figured with their factory default configurations. Details are provided in Chapter 3 of the *GateFlow User Manual* (see Documentation Required for Installation).

We recommend that before attempting any operational modifications of the default FPGA design, you should become very familiar with the board's performance when operated with the default design. Once you are comfortably familiar with the default operation, we recommend that your first project with the FPGA design kit should be to re–compile the default code with one very simple change (the contents of the read–only FPGA Revision registers), and re–configure the FPGA with the re–compiled con–figuration file. (Refer to Chapter 2 of the *GateFlow User Manual* for details.)

If you discover that you can use the entire default design for the FPGA, and simply need to add another function or two, Table 1–2 in Chapter 1 of the *GateFlow User Man–ual* will help you to determine how much of the FPGA's resources remain available for your use.

Documentation for This Product

Any of the documentation listed below that is not supplied with the Model 71760 can be found at www.pentek.com.

Product Documentation

Part No	Type / Description
800.71760	*Operating Manual - Model 71760 4-Channel A/D XMC Module*
801.71760	*Programmer's Reference - ReadyFlow Board Support Libraries for Model 71760*
807.71760	*User's Manual - Model 4953 Option 176 Design Kit for FPGA on the Model 71760*
809.7x760	*Supplemental Manual - Vendor Data Sheets for Model 7x760 Series Operating Manuals*
815.71660	*User's Guide - Model 4995A Option 166 Windows ReadyFlow BSP for Models 71660, 71661, 71662, and 71760*
816.71660	*User's Guide - Model 4994A Option 166 Linux ReadyFlow BSP for Models 71660, 71661, 71662, and 71760*

Other Technical Documentation

Catalogs:

- Pentek Product Catalog
- Product Selection Guide: http://www.pentek.com/selectguide/SelectGuide.cfm

Handbooks:

- Critical Techniques for High–Speed A/Ds In Real–Time Systems
- High–speed Switched Serial Fabrics Improve System Design
- Putting FPGAs to Work For Software Radio
- Software Radio Handbook

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